IN THE SPECIFICATION

Replace the paragraph beginning on page 1, line 24 with the following replacement paragraph:

Power supply sequence controllers enable system designers to meet the need for power sequencing in their designs. A programmable sequence controller may include programmable logic that a user programs according to the particular power sequence control desired. An example programmable sequence controller is disclosed in US Patent ~~Application~~ No. 6,735,706 ~~09/732,216 entitled "Programmable Power Management System and Method," filed December 6, 2000~~, which is hereby incorporated by reference in its entirety.

Please replace the paragraph beginning on page 3, line 7 with the following replacement paragraph:

The conventional approach to this problem is to provide two BSCAN headers on the circuit board: one connected to the sequencer and the other connected to a BSCAN chain containing the devices controlled by the sequencer. Once the sequencer has been programmed through one BSCAN header and is supplying power to the other devices, the devices are programmed or tested through the other BSCAN header. However, ~~this approach has the drawbacks that~~ the second BSCAN header increases costs and consumes scarce circuit board area.

Please replace the paragraph beginning on page 7, line 16 with the following replacement paragraph:

As seen in Figure 1, programmable sequencer 10 includes a 1:2 demultiplexer 40 controlled by a memory cell such as electrically erasable (EE) configuration memory cell 45.

LAW OFFICES OF MACPHERSON KWOK CHEN & HEID LLP
2403 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

Alternatively, memory cell may comprise a flip-flop. Depending upon the binary state of the signal 50 stored by cell 45, programmable sequencer 10 will either support primary BSCAN chain ~~210~~ 200 or secondary BSCAN chain 230 through BSCAN header 15. Should memory cell 45 comprise a flip-flop, the flip-flop may be configured to respond to a power-on reset command to select for primary BSCAN chain ~~210~~ 200. Demultiplexer 40 is positioned to receive the output from the last BSCAN cell 205 in programmable sequencer 10 in both primary BSCAN chain ~~210~~ 200 or second BSCAN chain 230 (it is the same BSCAN cell 205 for both chains). In addition, demultiplexer 40 is positioned within either chain past the path to the JTAG registers discussed earlier. Arbitrarily, demultiplexer 40 has been configured so that it will support primary BSCAN chain ~~210~~ 200 when signal 50 is in the high binary state (a logical "1"). Should signal 50 be in the high binary state, demultiplexer 40 will direct the signal from the last BSCAN cell 205 in programmable sequencer 10 to the TDO pin in BSCAN header 15. Alternatively, should signal 50 be in the low binary state (a logical "0"), demultiplexer 40 will direct the signal from the last BSCAN cell 205 in programmable sequencer 10 to the TDO_sec pin. As seen in Figure 2b, this pin exists within the secondary BSCAN chain ~~220~~ 230 signal path such that secondary BSCAN chain ~~220~~ 230 is supported when signal 50 is in the low binary state.

Please replace the paragraph beginning on page 8, line 12 with the following replacement paragraph:

Because both primary BSCAN chain ~~205~~ 200 and second BSCAN chain ~~220~~ 230 end at the TDO pin in BSCAN header 15, there is the possibility of TDO pin contention. Accordingly, demultiplexer 40 may couple to the TDO pin through a tri-state buffer 60. To provide the logic for its control, tri-state buffer 60 may be controlled by the output of an AND gate 65. In turn, AND gate receives signal 50 and an output 75 of the TAP state machine 70

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP
2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

discussed earlier. This output 75 of TAP state machine 70 will be a logical 1 whenever TAP state machine 70 is in the states that support signal flow through the TDO pin (such states will be denoted herein collectively as the BSCAN state). Thus, assuming TAP state machine 70 is in a state that supports this signal flow, the state of signal 50 will control whether tri-state buffer 60 is in the high impedance mode. The control of tri-state buffer 60 is such that when the output of AND gate 65 is a logical 1, tri-state buffer 60 is not in the high impedance mode. Conversely, when the output of AND gate 65 is a logical 0, tri-state buffer 60 is in the high impedance mode. A second tri-state buffer 80 coupled to the TDO_sec pin has a similar effect in the secondary BSCAN chain ~~220~~ 230 path.

Please replace the paragraph beginning on page 9, line 3 with the following replacement paragraph:

Tri-state buffer 80 is controlled by an AND gate 85. AND gate 85 receives ~~the~~ output 75 of TAP state machine 70 as well as an inverted version of signal 50 provided by an inverter 90. Thus, when TAP state machine 70 is in the BSCAN state and signal 50 is a logical 0, the output of demultiplexer 40 will flow through the TDO_sec pin within the signal path of secondary BSCAN chain ~~220~~ 230. Tri-state buffer 80 is controlled such that it is in the high-impedance state when the output of AND gate 85 is a logical 0.

Please replace the paragraph beginning on page 9, line 10 with the following replacement paragraph:

So long as the state of memory cell 45 is not changed during secondary BSCAN chain ~~220~~ 230 operation, tri-state buffer 60 will prevent any chance of TDO pin contention between programmable sequencer 10 and device 30. However, it is possible that the state of memory cell 45 might change during secondary BSCAN chain ~~220~~ 230 operation because of some

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP
2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

unexpected event. In such a case, programmable sequencer 10 may be driving the TDO pin to a first logical state while the output of secondary BSCAN chain ~~220~~ 230 from device 30 is driving the TDO to an opposite logical state, thereby causing TDO pin contention and faulty operation. The second pin embodiment that will be described next prevents such a pin contention possibility.

LAW OFFICES OF
MACPHERSON KWOK
CHEN & REID LLP

2402 Michelson Drive
Suite 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049